LESSON PLAN

Discipline: ELECTRICAL ENGG.	Semester: 5TH	Name of the Teaching Faculty: PARTHA SARATHI MALLICK
Subject: DIGITAL ELECTRONICS & MICROPROCESSOR (TH.3)	No. of days/ per week class allotted: 5	Semester From Date : 01/08/2023 to Date: 30/11/2023 No. of Weeks: 15
Week	**Class Day**	**Theory/ Practical Topics**
1st	1st	**BASICS OF DIGITAL ELECTRONICS :** Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	2nd	Binary addition, subtraction.
	3rd	Binary Multiplication and Division.
	4th	1's complement and 2's complement numbers for a binary number.
	5th	Subtraction of binary numbers in 2's complement method.
2nd	1st	Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	2nd	Importance of parity Bit.
	3rd	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	4th	Realize AND, OR, NOT operations using NAND, NOR gates.
	5th	Different postulates and De-Morgan's theorems in Boolean algebra.
3rd	1st	Different postulates and De-Morgan's theorems in Boolean algebra.
	2nd	Use Of Boolean Algebra For Simplification Of Logic Expression
	3rd	Karnaugh Map For 2,3,4 Variable.
	4th	Simplification Of SOP Logic Expression Using K-Map.
	5th	Simplification Of POS Logic Expression Using K-Map.
4th	1st	**COMBINATIONAL LOGIC CIRCUITS :** Give the concept of combinational logic circuits.
	2nd	Half adder circuit and verify its functionality using truth table.
	3rd	Half adder circuit and verify its functionality using truth table.
	4th	Realize a Half-adder using NAND gates only and NOR gates only.
	5th	Realize a Half-adder using NAND gates only and NOR gates only.
5th	1st	Full adder circuit and explain its operation with truth table.
	2nd	Realize full-adder using two Half-adders and an OR – gate and write truth table
	3rd	Realize full-adder using two Half-adders and an OR – gate and write truth table
	4th	Full subtractor circuit and explain its operation with truth table.
	5th	Full subtractor circuit and explain its operation with truth table.

Parthasarathi Mallick

6th	1st	Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	2nd	Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	3rd	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	4th	Working of Binary-Decimal Encoder & 3 X 8 Decoder.
	5th	Working of Two bit magnitude comparator.
7th	1st	**SEQUENTIAL LOGIC CIRCUITS :** Give the idea of Sequential logic circuits.
	2nd	State the necessity of clock and give the concept of level clocking and edge triggering,
	3rd	Clocked SR flip flop with preset and clear inputs.
	4th	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5th	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
8th	1st	Concept of race around condition and study of master slave JK flip flop.
	2nd	Give the truth tables of edge triggered D and T flip flops and draw their symbols
	3rd	Applications of flip flops.
	4th	Define modulus of a counter
	5th	4-bit asynchronous counter and its timing diagram.
9th	1st	Asynchronous decade counter.
	2nd	4-bit synchronous counter
	3rd	Distinguish between synchronous and asynchronous counters
	4th	State the need for a Register and list the four types of registers.
	5th	Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
10th	1st	**8085 A MICRO PROCESSOR:** Introduction to Microprocessors, Microcomputers.
	2nd	Architecture of Intel 8085A Microprocessor and description of each block.
	3rd	Architecture of Intel 8085A Microprocessor and description of each block.
	4th	Pin diagram and description.
	5th	Stack, Stack pointer & stack top.
11th	1st	Interrupts.
	2nd	Opcode & Operand.
	3rd	Differentiate between one byte, two byte & three byte instruction with example.
	4th	Differentiate between one byte, two byte & three byte instruction with example.
	5th	Instruction set of 8085 example.
12th	1st	Addressing mode.
	2nd	Addressing mode.
	3rd	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	4th	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5th	Timing Diagram for memory read, memory write, I/O read, I/O write
13th	1st	Timing Diagram for memory read, memory write, I/O read, I/O write
	2nd	Timing Diagram for 8085 instruction