DISCIPLINE: Electrical & Electronics Engg.	SEMESTER: 3rd Semester	NAME OF THE TEACHING FACULTY: Ms. Deepika Sarkar Lecturer -II in ETC ENGG.
SUBJECT: Digital Electronics(Th3)	NO OF DAYS/PER WEEK CLASSES ALLOTTED:3	SEMESTER FROM DATE: 14.07.2025 TO DATE: 15.11.2025 NO OF WEEKS:15

Week	Class Day	THEORY Topics
1st		I. Logic Gates
	1st	Basic logic gates: OR, AND, and NOT ,Truth tables ,Logic symbols Logic voltage levels ,Logic circuit design examples
	2nd	Integrated Circuits NOR, NAND, Exclusive OR, and Exclusive NOR gates..
	3rd	NOR and NAND gates used as inverters.
2nd	1ST	Fan-in and fan-out ,Termination of unused inputs AND and OR gates constructed from NAND and NOR gates
		II. Boolean Algebra
	2ND	Boolean operations (OR, AND, NOT), Representation of logic circuits by Boolean expressions.
	3RD	Laws of Boolean algebra: Double inversion: A"=A OR identities: A+0 = A, A+1=1, A+A=A, A+A'=1 AND identities: A.0=0, A.1=A, A.A=A, A.A'=0 ,Cumulative laws: A+B=B+A, A.B=B.A ,Associative laws:(A+B)+C=A+(B+C), (A.B).C=A.(B.C) ,Distributive laws: A+(B.C)=(A+B).(A+C), A.(B+C)=A.B+A.C
3rd	1st	DeMorgan's theorems :(A+B+C+...)'=A'.B'.C'...,(A.B.C...)'=A'+B'+C', Applications to logic circuit simplifications and design
	2nd	Equivalent logic gates, NAND and NOR implementations of logic circuits. Standard forms of Boolean expressions ,
	3rd	Sum-of-products (SOP) ,Product-of-sums (POS) ,Karnaugh mapping.
		III. Combinational Logic Circuits
4th	1ST	Half adder ,Full adder ,Half Subtractor , Full Subtractor,.
	2ND	4 bit adder
	3RD	Multiplexer (4:1) ,De- multiplexer (1:4)
5th	1ST	Decoder, Encoder
	2ND	Digital comparator (3 Bit)
	3RD	Seven segment Decoder
		IV Latches & Flip-Flops
6th	1ST	Basic latches NOR latch ,NAND latch , Example uses of latches
	2ND	Gated latches ,Gated S-R latch , Gated D-latch
	3RD	Flip-flops: Master-slave and edge-triggered principles
7th	1ST	S-R flip-flop
	2ND	D-type flip-flop

	3RD	J-K flip-flop , T-type flip-flop , Flip-flop timing diagrams
		V.Counters
8th	1ST	Circuit diagram and working principle of Binary counters
	2ND	up-down counter (circuits, truth tables, and timing diagrams)
	3RD	Asynchronous counters and ripple counter, Synchronous counters
9th	1ST	Decade counter
	2ND	Module–n counter and its combinations , Divide-by-n counters obtained from truncated binary sequences
	3RD	Synchronous counter design using D-type flip-flops
10th	1ST	Synchronous counter design using J-K flip-flops
		VI. Shift Registers
	2ND	Circuit diagram, truth tables, and timing diagrams of Shift Registers
	3RD	Serial input shift register
11th	1ST	Serial/parallel load shift register
	2ND	Shift register counters. Ring counter
	3RD	Self-starting ring counter , Johnson counter
		VII.Semiconductor Memories
12th	1ST	Define the terms ROM, RAM, PROM, EPROM
	2ND	Draw a typical memory cell
	3RD	Design a small diode matrix ROM to serve as a code converter.
	1ST	Design and draw the logic diagram of a specified size memory system
	2ND	Operating principle of dynamic memory
	3RD	Advantages and disadvantages of dynamic memory vs. static memory
14th	1st	Difference between dynamic memory vs. static memory
		VIII. Sequential Circuit Design
	2nd	Combinational vs. Sequential circuits
	3rd	Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
15th	1ST	Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	2ND	Finite state machines- Concept only
	3RD	Doubt clearing class

Lecturer 14.07.25

HOD 14.07.25

Principal 14/7/25