DISCIPLINE: Electrical & Electronics Engg.	SEMESTER: 4th Semester	NAME OF THE TEACHING FACULTY: Ms. Deepika Sarkar Lecturer -II in ETC ENGG.
SUBJECT: MICROPROCESSOR AND MICROCONTROLLER (TH-03)	NO OF DAYS/PER WEEK CLASSES ALLOTTED:3	SEMESTER FROM DATE: 22.12.2025 TO DATE: 18.04.2026 NO OF WEEKS:15

Week	Class Day	Topics
		1.Digital Fundamentals
1st	1st	Number Systems – Decimal, Binary, Octal
	2nd	Hexadecimal, 1's and 2's complements
	3rd	Codes – Binary, BCD, Excess-3, Gray, Alphanumeric codes.
2nd	1ST	Boolean theorems, Logic gates and truth tables, Universal gates
	2ND	Sum of products and product of sums, Minterms and Maxterms.
	3RD	Karnaugh map Minimization and Quine-McCluskey method of minimization.
3rd	1st	ASSIGNMENT
	2nd	CLASS TEST
		2. Combinational & Synchronous Sequential Circuits
	3rd	Design of Half and Full Adders,
4th	1st	Half and Full Subtractors ,
	2nd	Binary Parallel Adder -Multiplexer, Demultiplexers,
	3rd	ASSIGNMENT
5th	1st	Decoders and Priority Encoder.
	2nd	Flip flops – SR, JK, T, D
	3rd	design of clocked sequential circuits
6th	1ST	Design of Counters- Shift registers, Universal Shift Register.
	2ND	CLASS TEST
		3. Asynchronous Sequential Circuits And Memory Devices
	3RD	Stable and Unstable states, output specifications,
7th	1ST	cycles and races, state reduction,
	2ND	race free assignments, Hazards, Essential Hazards,
	3RD	Pulse mode sequential circuits, Design of Hazard free circuits.
8th	1ST	Basic memory structure – ROM -PROM – EPROM – EEPROM –EAPROM, RAM
	2ND	Static and dynamic RAM – Programmable Logic Devices
	3RD	Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA).
9th	1st	ASSIGNMENT
	2nd	CLASS TEST
		4. 8085 Processor
	3rd	Hardware Architecture
10th	1ST	pin diagram
	2ND	– Functional Building Blocks of Processor
	3RD	Memory organization
11th	1st	I/O ports and data transfer concepts
	2nd	Timing Diagram

	3rd	Interrupts.
12th	1ST	ASSIGNMENT
	2ND	CLASS TEST
		5. Programming Processor
	3RD	Instruction – format and addressing modes
13th	1st	Assembly language format
	2nd	Data transfer,
	3rd	data manipulation & control instruction
14th	1ST	Programming: Loop structure with counting & Indexing
	2ND	Look up table
	3RD	Subroutine instructions – stack
15th	1st	8255 architecture and operating modes
	2nd	ASSIGNMENT
	3rd	CLASS TEST

Lecturer 22.12.25

HOD 22.12.25

Principal 22/12/25